March 16, 2004

INFORMATION DISCLOSURE STATEMENT letter

To Whom It May Concern:

The following documents are included in form PTO/SB/08A Information Disclosure Statement by Applicant (a pro se filer) as a bibliography for the application having the following title and applicant.

Title: Comparing Circuits for Time-to-Threshold A/D Conversion in Digital Imaging Arrays

Applicant: Charles D. Murphy

Here, the documents are discussed as they relate to the specification and claims of the application.

The present invention proposes CMOS logic gates (i.e. with both p-type and n-type transistors) as threshold detectors in digital imaging arrays which use time-to-threshold A/D conversion. In such a setting the circuits have an analog input and provide a digital output indicating when the input passes an implicit threshold voltage. With chip space at a premium in many CMOS image sensor arrays, CMOS logic gates with minimum-size transistors are possible in the present invention.

In much of the prior art, comparison of analog signals is accomplished using circuits with explicit signals, such as two-input comparators. Two-input comparators are widely used in many types of A/D converters. The fourth edition of The Art of Electronics by Paul Horowitz and Winfield Hill discusses various types of prior art A/D converters on pages 621-630. A typical prior art flash converter design using comparators appears in figure 9.49 on page 621.

The prior art work of K. Choi and colleagues from Penn State University proposed inverters as comparators in flash converters they describe as "threshold inverter quantizer" (TIQ) converters. Instead of having a resistor ladder generating explicit reference voltages, the inverters are created with differing transistor gate size ratios. This creates a set of implicit reference voltages. Drawbacks of the approach are the need for accurate matching of the various sizes as well as inverter count and average size that increase exponentially with precision. (Applicant notes a large number of publications by Choi and his colleagues, but provides only a hard copy of "A 11-GSPS CMOS Flash A/D Converter for System-on-Chip Applications" by J. Yoo, K. Choi, and A. Tangel presented at the IEEE Computer Society Workshop on VLSI 2001, April 19-20, 2001.)

However, in the art of time-to-threshold A/D converters, which are particular to and exploit digital imaging arrays with sensors configured as integrators, there are no examples of inverters or other digital logic gates used for threshold detection.

U.S. Patent 6,587,145 issued to A. Hou on July 1, 2003 and entitled IMAGE SENSORS GENERATING DIGITAL SIGNALS FROM LIGHT INTEGRATION PROCESSES describes time-to-threshold A/D conversion with two-input comparators as threshold detectors. Each comparator consists of two n-type transistors, one of which receives a

pinned photodiode output at its gate while the other receives an explicit externally-supplied reference threshold level. The two transistors compete for control of a common output node, with the winner pulling that node toward reference output levels.

U.S. Patent 5,461,425 issued to B. Fowler and A. El Gamal on October 24, 1995 and entitled CMOS IMAGE SENSOR WITH PIXEL LEVEL A/D CONVERSION describes a digital imaging array in which each sensor has a dedicated A/D converter. The A/D converters suggested are general purpose in that they don't exploit the nature of the acquired signal (i.e. that it's proportional to the cumulative incident energy since reset).

U.S. Patent 5,479,208 issued to F. Okumura on December 26, 1995 and entitled IMAGE SENSORS AND DRIVING METHOD THEREOF describes a type of time-to-threshold A/D conversion in which a sensor output change is amplified then stored and provided as one input to a two-input comparator. Subsequently, a time-varying reference signal is generated, amplified by the same amplifier, and provided as the other input of the comparator. The comparator output switches when the time-varying reference signal reaches a "threshold" of the held sensor output change plus or minus the comparator's input offset. This approach is quite similar to prior art A/D conversion techniques such as single-slope or dual-slope conversion and suffers from the usual drawbacks of high-precision reference signal generation at reasonably high speeds (e.g. steep linear ramp segments are highly nonlinear due to dielectric absorption).

U.S. Patent 5,479,208 includes the following statement on column 6 of the specification, lines 22 through 28:

> Further, in this embodiment, although the system is compose of the analog circuits, in particular, almost all of these can be replaced with digital circuits. For example, the sample hold circuit can be replaced with an A/D (analog-digital) converter and a latch circuit and the comparator is replaced with a comparator composed of a logic. [SIC] The signal converter can, of course, be digitized as described above.

In the figures of U.S. Patent 5,479,208, analog signal comparison is clearly presented as accomplished using a two-input comparator. For instance, the signal detector 6 in Fig. 2 is illustrated in Fig. 3 as being composed of a sample hold circuit 7 feeding one input of a (two-input) comparator 8. In Fig. 6, the signal detector is presented with A/D converter 11 alternately processing a sensor output passed through amplifier 5 and a reference voltage passed through amplifier 5. In Fig. 7, amplifier 5 is depicted as a single n-type MOS transistor.

In the specification, column 3 lines 49 through 55 describes "digitization" of the idea of U.S. Patent in the form of A/D conversion of two analog signals with digital comparison of the results (e.g. the approach of Fig. 6). The Applicant submits that the reference of column 6 lines 22 through 28 is to this "digitization" rather than to a digital logic gate treated as a comparator with an implicit threshold.

U.S. Patnet 6,642,503 issued on November 4, 2003 to R.K. Kummaraguntla, Z.J. Chen, and J.G. Harris and entitled TIME DOMAIN SENSING TECHNIQUE AND SYSTEM ARCHITECTURE FOR IMAGE SENSOR describes time-to-threshold A/D conversion in digital imaging. Comparison is accomplished with a two-input comparator (e.g. Fig. 4 and discussion of comparator 28, Fig. 9 and discussion of shared comparator 70).

Several other U.S. patents describe various aspects of time-to-threshold A/D conversion in digital imaging.

Related U.S. Patent 6,559,788 issued on May 6, 2003 and entitled PARALLEL AND SHARED PARALLEL ANALOG-TO-DIGITAL CONVERSION FOR DIGITAL IMAGING. The related patent included various proposed sets of shared components, dedicated components, count recording devices, variable-frequency counters, and other useful structures.

U.S. Patent 5,650,643 issued to K. Konuma on July 22, 1997 and entitled DEVICE USED FOR RECEIVING LIGHT USED IN CCD IMAGE SENSOR OR THE LIKE describes time-to-threshold A/D conversion with a dedicated counter for each sensor, allowing a single master clock signal to be passed into the array. Disadvantages of the approach are massive redundancy of counters and a corresponding high cost in terms of chip area and power consumption.

U.S. Patent 6,680,498 issued to R. Guidash on January 20, 2004 and entitled CMOS IMAGE SENSOR WITH EXTENDED DYNAMIC RANGE describes a system in which two measurements are taken with differing exposure times. It does not propose a time-to-threshold technique but does discuss other digital imaging array techniques, notably the multiple-measurement approach of O. Yadid-Pecht and colleagues and the reset-during-integration approaches of J. Huppertz, S. Decker, and their respective colleagues.

U.S. Patent 6,069,377 issued to W.E. Prentice and R. Guidash on May 30, 2000 and entitled IMAGE SENSOR INCORPORATING SATURATION TIME MEASUREMENT TO INCREASE DYNAMIC RANGE describes the use of both a prior art fixed-time-exposure measurement and a time-to-threshold measurement. However, both signals (cumulative sensor output response and elapsed time) are stored as analog signals and passed out of the array for A/D conversion.

U.S. Patent 6,307,195 issued to R. Guidash on October 23, 2001 and entitled VARIABLE COLLECTION OF BLOOMING CHARGE TO EXTEND DYNAMIC RANGE is similar to U.S. Patents 6,680,498 and 6,069,377 discussed above, with blooming charge (e.g. overflow due to saturation) measurements in addition to sensor output change measurements. The measurements occur after different exposure times.

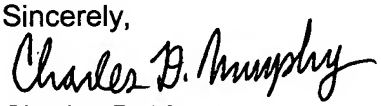
U.S. Patent 6,552,745 issued to F.A. Perner on April 22, 2003 and entitled CMOS ACTIVE PIXEL WITH MEMORY FOR IMAGING SENSORS describes a type of time-to-threshold measurement. As with U.S. Patent 5,479,208 discussed above, a sensor output is compared to a time-varying reference signal (e.g. a ramp or other waveform segment), with a comparator output swing indicating threshold crossing. U.S. Patent 6,552,745 also suggests array-internal digital memory circuits and double sampling via processing of a known reference threshold level.

The present invention proposes CMOS inverters, other CMOS logic gates, and CMOS logic-type gates (e.g. the n-type pull-up, p-type pull-down architecture) as threshold detectors with implicit thresholds rather than explicit thresholds, in time-to-threshold A/D converters for digital imaging systems.

While the prior art includes various types of time-to-threshold A/D converters in digital imaging systems and CMOS inverters as comparators in general purpose flash A/D converters, I, the pro se applicant and inventor of the present invention have been unable to find any prior art closely similar to the material of the present invention. To the best of my knowledge, the ideas of the present invention are new and deserving of patent protection.

This concludes this INFORMATION DISCLOSURE STATEMENT letter.

Sincerely,



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(Use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Charles Douglas Murphy
Art Unit	
Examiner Name	
Attorney Docket Number	

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 6587145	07-01-2003	A. Hou	
		US- 5461 425	10-24-1995	B. Fowler & A. El Gamal	
		US- 5479 208	12-26-1995	F. Okumura	
		US- 6642503	11-04-2003	R.K. Kummaraguntla et al.	
		US- 6559 788	05-06-2003	C.D. Murphy	
		US- 5650683	07-22-1997	K. Konuma	
		US- 6680498	01-20-2004	R. Guidash	
		US- 6069377	05-30-2000	W.E. Prentice & R. Guidash	
		US- 6307195	10-23-2001	R. Guidash	
		US- 6552 745	04-22-2003	F.A. Perner	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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(Use as many sheets as necessary)

Sheet 2 of 2

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	CHARLES DOUGLAS MURPHY
Art Unit	
Examiner Name	
Attorney Docket Number	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		PAUL HOROWITZ + WINFIELD HILL, The Art of Electronics, pages 621-630, 4th edition, 1994, Cambridge University Press, New York	
		JENCHEOL YOO, KYUSUN CHOI, + ALF TANGEL, "A 1GSPS CMOS Flash Converter for System-on-Chip Applications", IEEE Computer Society Workshop on VLSI, April 19-20, 2001.	

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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